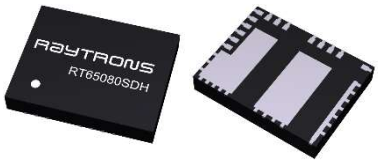
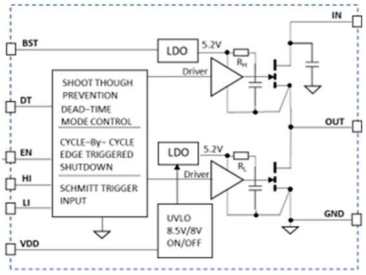
Features

- Complete $R_{DSON,MAX}$=85mΩ Half-Bridge GaN-Based power stage with QFN System-In-Package.
- Maximum Drain to Source Current 30A @ Tc=25°C
- GaNCooling™ technology by Bottom Side Cooling
- Low FOM for low Switching Loss
- Complete solution within 12.7mm x 10mm x 1.95mm Footprint
- Dual PWM operation and Dead Time Setting
- Fast Rise/Fall Times and low Propagation Delay
- Reverse Current capability and Zero Q_{RR}
- Moisture Sensitivity Level 3 (260°C)

QFN 12.7x10mm² System in Package (SiP)



Simplified Schematic



Typical Applications

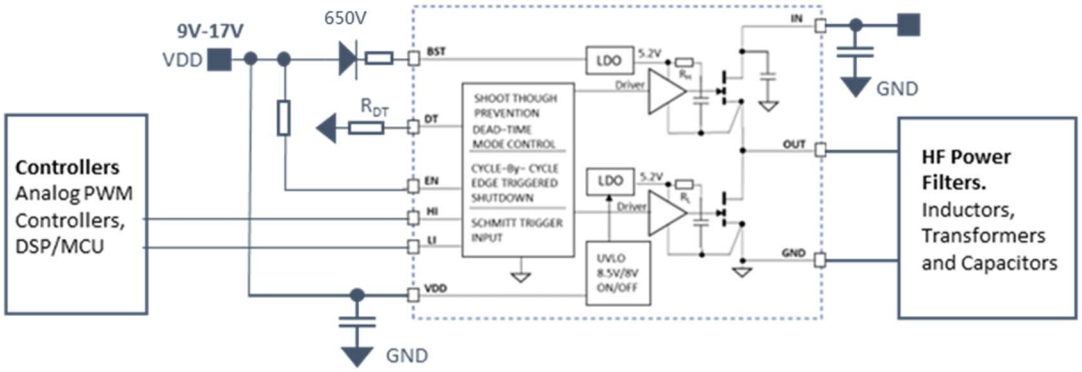
- Compact AC/DC Power Supplier
- Totem Pole PFC, LLC DC/DC Topologies
- Motor Drive Inverter

Description

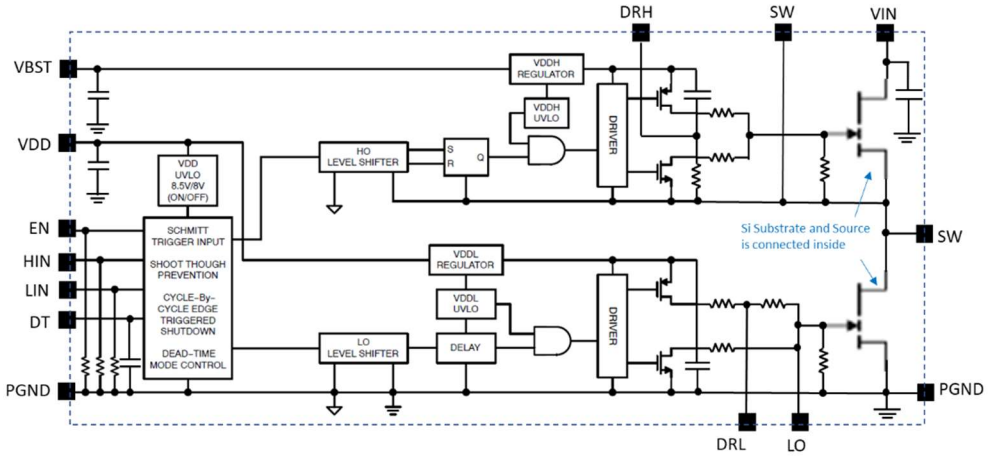
RT65 CIPS (Complete Integration Power Stage) Series are Fully Integrated GaN Half-Bridge power stages for multiple Applications in Fast Charger, High Power Density Switching Power, and Consumer segments. These CIPS are small-footprint, easy-to-design, and serve as a “drop-in” solution for board power. RT65 CIPS Series couples world-class GaN performance to Raytrons GaNCooling™ embedded modules that GaNCooling™ technology is a patented construction embeds all components without using bond wires, minimizing inductance, achieving ultra-low voltage spikes on gate and switch nodes, and minimizing RFI. The high dV/dt immunity, <1nH loop inductance and low thermal resistance to provides highest level of Power Density allowing designer simple, and quick to design high power density product.

Typical Application Circuit

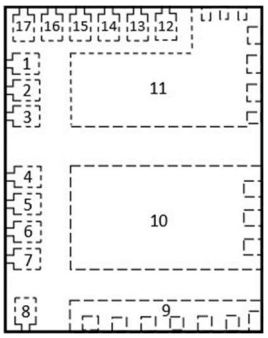
RT65060SDH can be designed in high power density power supply, including LLC, PWM half-bridge converter, totom ploe PFC, Motor Driver and so on. Power loop (loop impedance from IN capacitor to PGND) PCB layout is critical, designer can refer to the PCB layout consideration section to enhance thermal performance easily.



Block Diagram



Pinout Table



Pinout		I/O Type	Description and Operation
#	Name		
1,11	PGND	Power GND	Connect to PCB Ground thru multiple Via's
2	VDD	Supply	Low side bias voltage. 9V to 17V operating rang.
3,8	NC	-	No Connection
4	VBST	Supply	Floating high side bias voltage
5,6,10	SW	Power Output	Half-Bridge power stage output (switching node)
7	DRH	Input	Option. Parallel a resistor between HDR and SW to speed up dv/dt falling time at SW node if necessary.
9	VIN	Power Input	Supply voltage to half-bridge power stage (buck-mode)
12	DRL	Input	Option. Parallel a resistor between DRL and LO to speed up dv/dt rising time at SW node if necessary
13	LO	Output	Low Side Gate
14	DT	Input	Dead time adjustment / mode selection
15	LIN	Input	Logic input for low−side gate driver output
16	HIN	Input	Logic input for high−side gate driver output
17	EN	Input	Logic input for disabling the driver. Pulling the EN pin above 2.5 V maximum, enables the outputs, placing the module into an active ready state.

Absolute Maximum Ratings (T_{CASE} = 25 °C)

Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

- VIN to GND, VIN to SW, SW to GND ---------- 630V
- VDD to GND ---------- 18V
- Logic Input (HIN, LIN, EN) and DT ---------- VDD+0.3V
- LDR, LIN, HIN to GND ---------- 18V
- HDR, BST to GND ---------- 640V

Thermal Characteristics

The Surface Mount Device (SMD) with Bottom-side Cu Pads for Surface Mount PCB attach. $R_{\_JUNC-AMB}$ value based on recommended Via Pattern with multi-layer FR4 PCB. No Airflow (zero LFM) and no Top-side Heat Sink required to meet $R_{\_JUNC-AMB}$ (Conduction Heat Transfer). It is much more effective and competitive thermal design.

- Maximum Thermal Resistance (Junction to Board), R_{Θ_JB}, ---------- 1.0 °C/W
- Thermal Resistance (Junction to Ambient), R_{Θ_JA}, ---------- 8.4 °C/W
- Maximum Soldering Temperature (MSL3 rated), T_{Solder} ---------- 260°C

Normal Operation Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Nominal VIN Range	$VIN_{\_Nom}$	6.2		600	V	
Nominal SW Range	$SW_{\_Nom}$	0.9		600	V	
Nominal VDD Range	$VDD_{\_Nom}$	9	12	17	V	
Nominal I/O Voltage	V_{IO_Nom}	2.5		17	V	
Nominal BST Range	$VBST_{\_Nom}$			SW+17	V	
Continuous I_{DS}	I_{DS_Nom}		30		A	T_{JUN}=25°C
Pulsed I_{DS}	I_{DS_Pulse}		58		A	T_{JUN}=25°C, T_{PULSE}=10us
Operating Temp	$T_{OPER.}$	-40		105	◦ C	

Electrical Specifications (T_{JUN}=25 Degrees of C)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-Source On Resistance	$R_{DS,ON}$		65	85	m Ω	H/S and L/S GaN Devices
Source-Drain Forward Voltage	V_{SD}		2.6		V	I_S = 8A, V_{GS} = 0 V
Input Capacitance	C_{ISS}		240		pF	V_{DS} = 400 V, V_{GS} = 0 V
Reverse Transfer Capacitance	C_{RSS}		1			
Output Capacitance	C_{OSS}		103			
Source-Drain Recovery Charge	Q_{RR}		0		nC	
Gate Resistance	R_G		3.5		Ω	
Bootstrap capacitance	C_{BST}	80	100		nF	DC-Bias=0V
VDD capacitance	C_{VCC}	80	100		nF	DC-Bias=0V
Switching Frequency	F_{SW}	18		200	kHz	Under CCM Operation
High Level Input Voltage Threshold	V_{INH}	-	-	2.5	V	

Low Level Input Voltage Threshold	V_{INL}	1.2	-	-	V	
Input Logic Voltage Hysteresis	$V_{IN,HYS}$		0.5		V	
Input Pull−down Resistance	R_{IN}		333		kΩ	V_{HIN} = V_{LIN} = 5 V
Minimum Dead−Time Control Voltage	$V_{DT,MIN}$	0.45	0.6	0.75	V	R_{DT} = 30 kΩ
	$t_{DT,MIN}$	22	30	38	ns	
Maximum Dead−Time Control Voltage	$V_{DT,MAX}$	3.1	4.0	4.8	V	R_{DT} = 200 kΩ
	$t_{DT,MAX}$	160	200	240	ns	
Dead−Time Disable Threshol	$V_{DT,0}$	0.35	0.4	0.45	V	Cross conduction prevention active
High− & Low−Side Overlap Enable Threshold	$V_{DT,OLE}$	5.5	6.0	6.5	V	Cross conduction prevention disabled
Propagation Delay	$T_{PD(H,L)}$			35	nsec	HI to SW, VIN=400V, and 2A I_{OUT}
Thermal Shunt Down	TSD	150			oC	Guaranteed by design, , is not tested in production.
Hysteresis of Thermal Shutdown	T_{HYS}		50		oC	
VDD Undervoltage-Lockout	$VDD_{,UVLO}$	8.0	8.5	9.0	V	VDD = Sweep
VDD Threshold Hysteresis	$VDD_{,HYS}$		0.5		V	
SW Rising Time	$T_{SW,R}$			3.5	nsec	VIN=400V, F_{SW}=100kHz and 2A I_{OUT}
SW Falling Time	$T_{SW,F}$			5.5	nsec	

Application Specifications

VDD UVLO (Undervoltage-Lockout):

When VDD pin detects a starting threshold voltage level of 8.5V (typical) on a rising edge, the device will go from its 1.5mA to 2.5mA supply current state to normal operation and <150uA Quiescent VDD supply current. making it well suited for +12 V bias rails. A typical start-up waveform as below: (yellow: VB, blue: VDD and pink: SW)

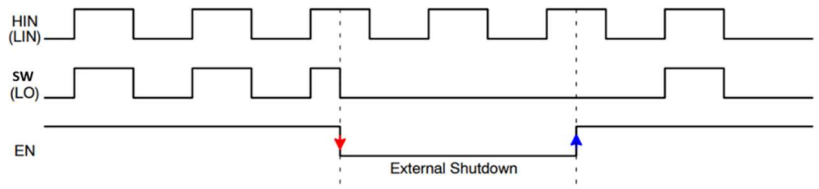
Input (HIN, LIN)

Both independent PWM inputs are Schmitt trigger, Transistor−Transistor Logic (TTL) compatible and are internally pulled low to GND such that each corresponding driver input is defaulted to the inactive (disabled) state. The TTL input thresholds provide buffer and logic level translation functions capable of operating from a variety of PWM signals up to VDD of the internal driver. TTL levels permit the inputs to be driven from a range of input logic signal levels for which a voltage greater than 2.5 V

maximum is considered logic high. Both input thresholds meet industry−standard, TTL−logic defined thresholds and are therefore independent of VDD voltage. A typical hysteresis voltage of 0.5 V is specified for each driver input. For optimal high−speed switching performance, the driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/us or faster, so a rise time from 0 to 3.3 V should be 550 ns or less.

Enable (EN)

Enable (EN) is internally pulled low to GND so the driver is always defaulted to a disabled output status. S Pulling the EN pin above 2.5 V maximum, enables the outputs, placing the RT65080SDH into an active ready state. It is recommended to connect the EN pin to VDD through a 1 kOhm (or less) pull−up resistor. For applications where the EN pin is actively controlled, the EN pin can be driven direct but should be bypassed with a 10 nF decoupling capacitor. If EN is pulled low during normal operation, the driver outputs are immediately disabled, even terminating an active HIN or LIN pulse mid–cycle during the on−time. When EN is toggled high, during normal operation, a cycle−by−cycle, edge−triggered logic function is employed to prevent shortened, erroneous control pulses from being processed by the output. This behavior is highlighted in below, where EN transitions high at the same time the HIN (or LIN) input pulse is high.



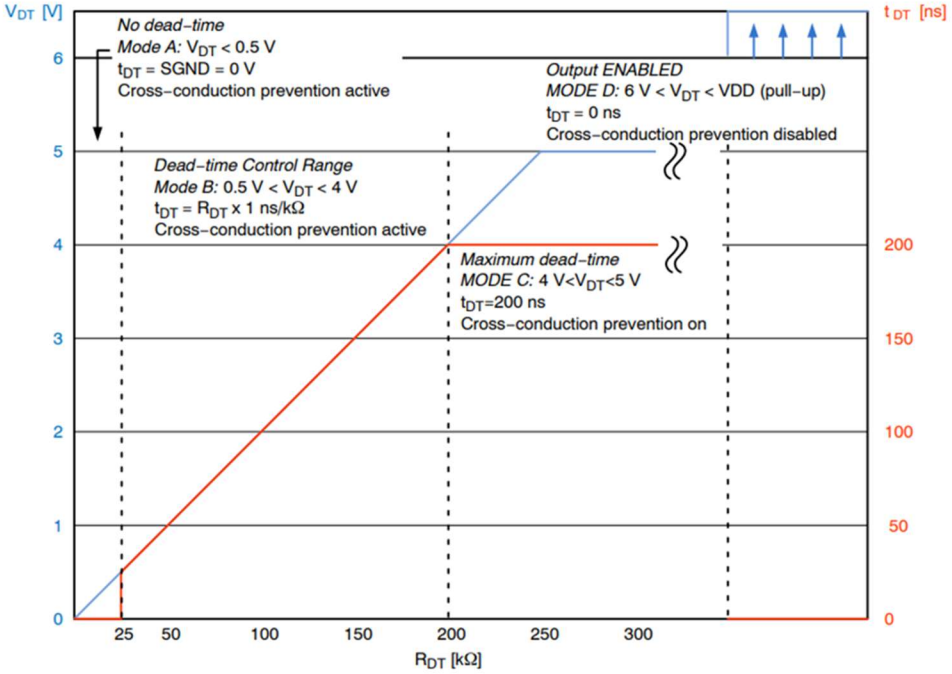
Dead−Time Control (DT)

The R_{DT} resistor should be placed directly in RT pin as close as possible. Internal driver offers four unique mode settings to utilize dead−time in such a way to be fully compatible with any control algorithm.

- Mode A：Connect DT to GND
  - DT pin voltage, V_{DT} is less than 0.5V typical (R_{DT}=0Ω). the DT programmability is disabled.
  - HIN and LIN are overlapping by X ns, then X ns of dead−time is automatically inserted. anti−cross−conduction protection is enabled
  - HIN and LIN have greater than 0 ns of dead−time, then the dead−time is not modified and is passed through to the output stage as defined by the controller.

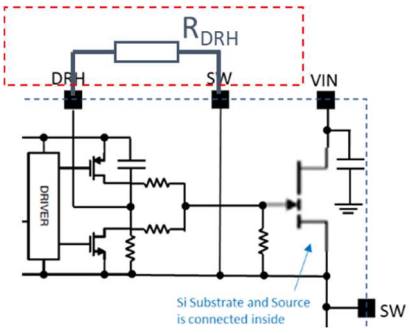
  This type of dead−time control is preferred when the controller will be making the necessary dead−time adjustments but needs to rely on the internal driver's dead−time control function for anti−cross−conduction protection.
- Mode B：Connect a 25 kΩ < R_{DT} < 200 kΩ Resistor from DT to GND
  - DT pin voltage, V_{DT}, for R_{DT} is 0.5V< V_{DT} < 4V
  - The amount of desired dead−time can be programmed via the dead−time resistor, R_{DT}, between the range of **25 kΩ < R_{DT} < 200 kΩ** to obtain an equivalent dead−time, proportional to R_{DT}, in the range of **25 ns < t_{DT} < 200 ns**.
- Mode C：Connect a 249 kΩ Resistor from DT to GND
  - DT pin voltage, V_{DT}, for assuring t_{DT} = 200 ns is 4 V<V_{DT}< 5V.
  - Connect a 249 kΩ resistor between DT and GND to program the maximum dead−time value of 200ns. The control voltage range, V_{DT}, for assuring t_{DT} = 200 ns is 4 V<V_{DT}< 5V.
- Mode D：Connect DT to VDD
  - DT pin voltage, V_{DT} is greater than 6V (pulled up to V_{DD} through 10 kΩ resistor) anti−cross−conduction protection is disabled, allowing the output signals to overlap.

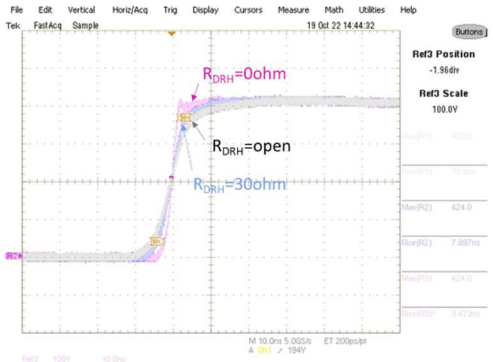
- As cross conduction can potentially damage RT65080SDH



Adjustable Turn-on dV/dt Control

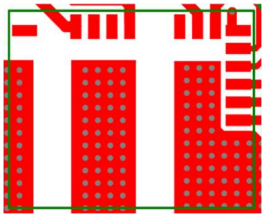
To reduce switching loss in high frequency hard switching operation, parallel a resistance between HDR and SW (or LDR and LO) can speed up dV/dt at switching node to increase efficiency.





PCB Layout Considerations：

Thanks for power loop decoupling capacitors are integrated, RT65080SDH is unlike to other GaN power products that needs to much take care PCB layout, only **utilize multiple Via's to connect PCB power and GND planes to the Module Pads to enhance thermal performance.** RT65080SDH is designed for PCB layout easily.

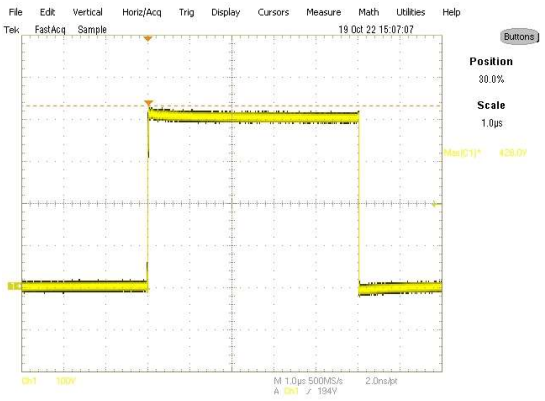


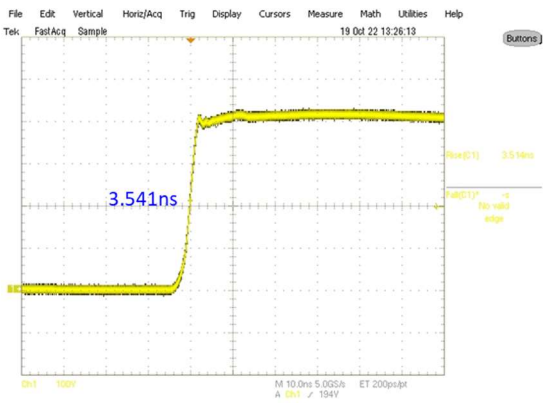
Thermal enhanced PCB layout design：Utilize multiple Via's to connect PCB power and GND planes to the Module Pads

Switching Waveforms：

Thanks for power loop decoupling capacitor is integrated inside, RT65080SDH have an ultra-low power loop inductance (<0.5nH), a clean switching waveforms will be presented even doesn't need to consider PCB layout rules.

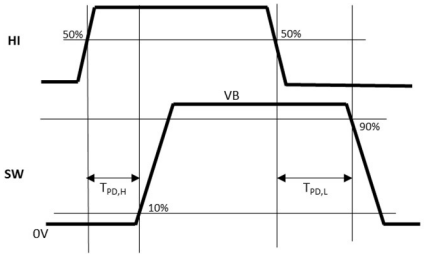
VIN=400V, Duty Cycle=50%, F_{SW}=100kHz, loading=2A. dv/dt=90V/ns (R_{DRH}=open)



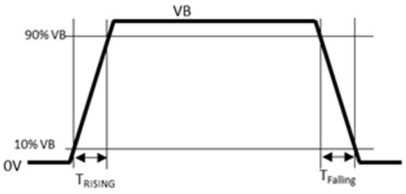


Propagation delay and rise/fall time definitions

a. Propagation Delay, $T_{PD,H}$ and $T_{PD,L}$

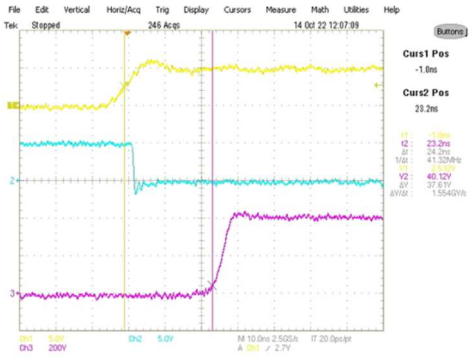


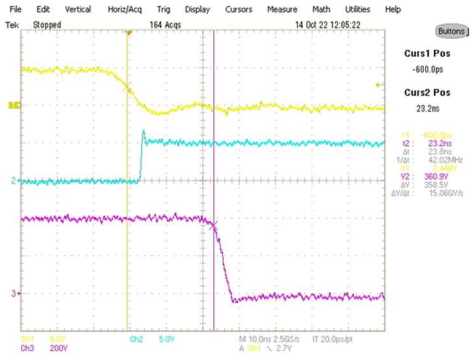
b. Rising/Falling Time, T_{Rising} and $T_{Falling}$



Propagation delay waveforms：

$T_{PD,H}$ and $T_{PD,L}$~25nsec. (Yellow：HI, Light Blue：LI and Purple：SW)



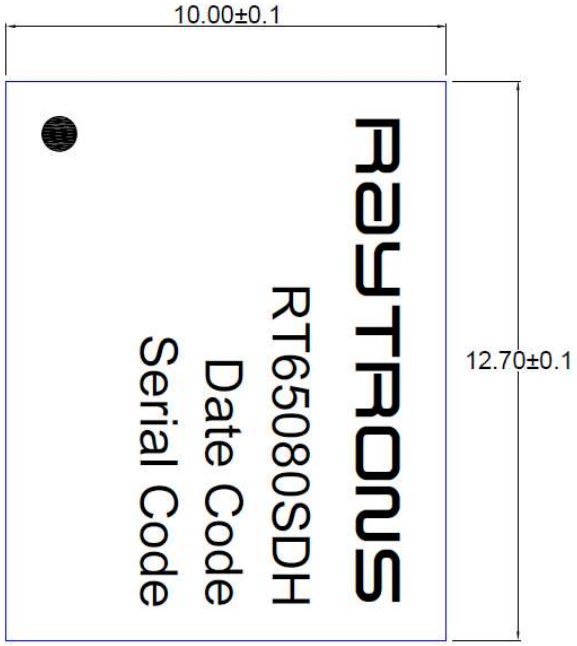


400V/200V Open Loop Buck/Boost Evaluation Board:

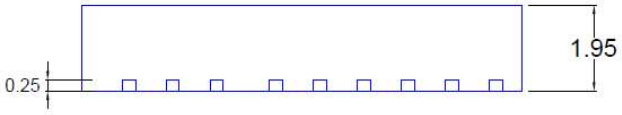
The Evaluation Board with 600V GaN-Based SMT power stage module provides a complete 400V step Up/down converter which can be used to evaluate efficiency & power density for use in applications such as bridgeless totem pole PFC, LLC converter power stage Class D audio systems, and inverter. The Buck/Boost Evaluation user manual is available.

Package Outline： (QFN-SiP - 2 mm max height)

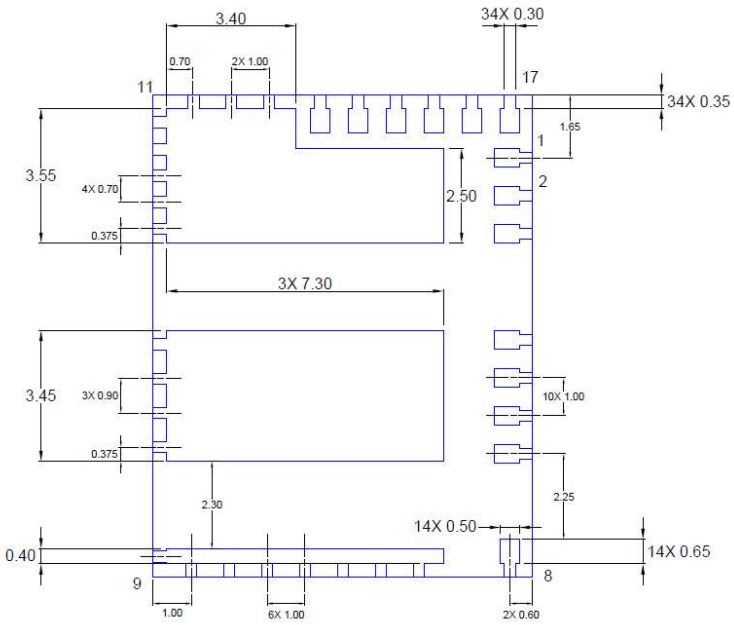
TOP VIEW



SIDE VIEW

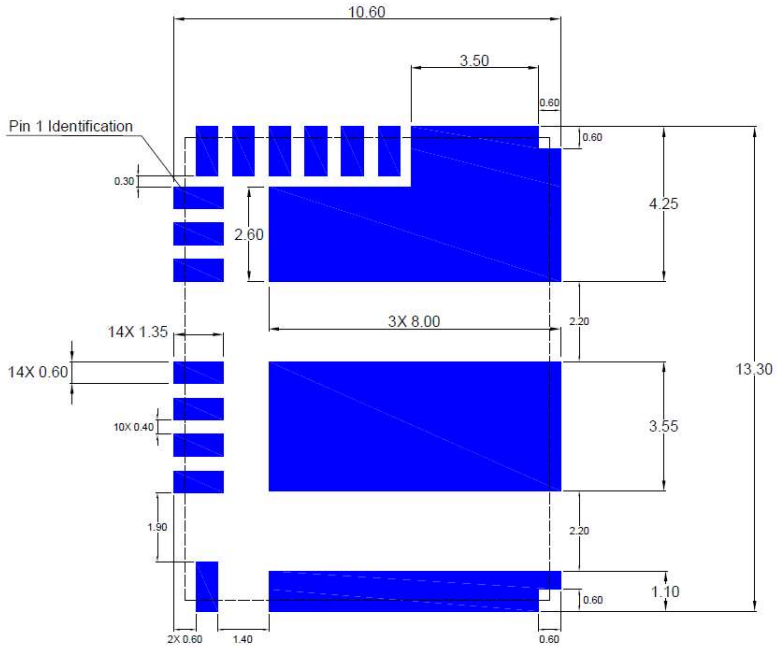


BOTTOM VIEW



※All dimensions are in units mm.
※General tolerence is 0.05 mm unless otherwise noted.

Example Board Layout and Stencil Design：



RECOMMENDED LAND PATTERN

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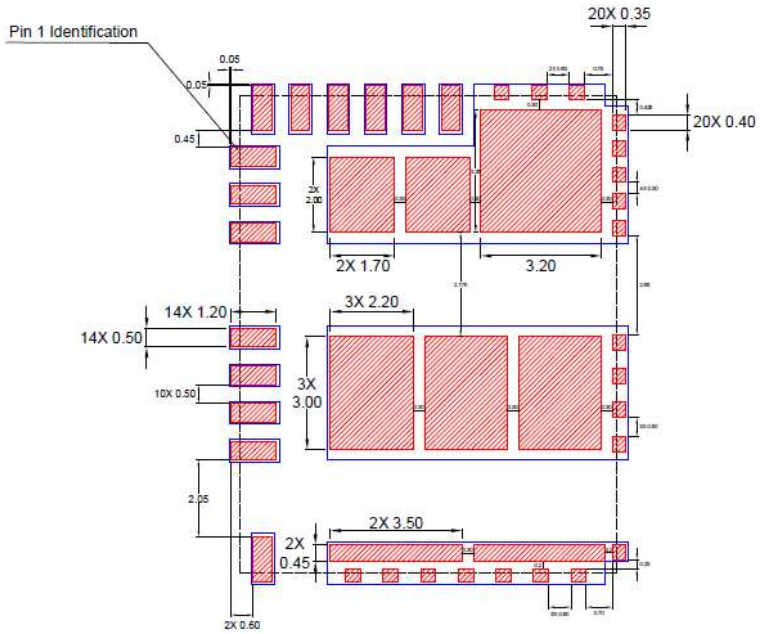

RECOMMENDED SOLDER PATTERN

※All dimensions are in units mm.
※51%~74% printed solder coverage by area under package.