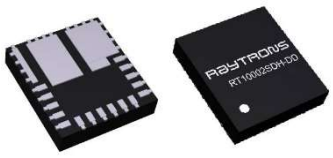
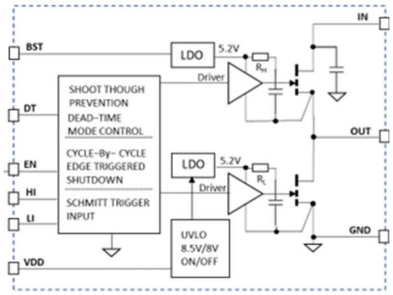
Features

- Complete R_{DSON}=2.4mΩ (02) and 5.6 mΩ (05) Half-Bridge GaN-Based power stage with QFN System-In-Package.
- Maximum Drain to Source Current
  RT10002SDH-DD - 60A
  RT10005SDH-DD - 16A
- GaNCooling™ technology by Bottom Side Cooling
- Low FOM for low Switching Loss at 1MHz+
- Complete solution within 10mm x 9mm x 1.95mm Footprint
- Dual PWM operation and Dead Time Setting
- Fast Rise/Fall Times and low Propagation Delay
- Reverse Current capability and Zero Q_{RR}
- Moisture Sensitivity Level 3 (260°C)

QFN 10x9mm² System in Package (SiP)



Simplified Schematic



Typical Applications

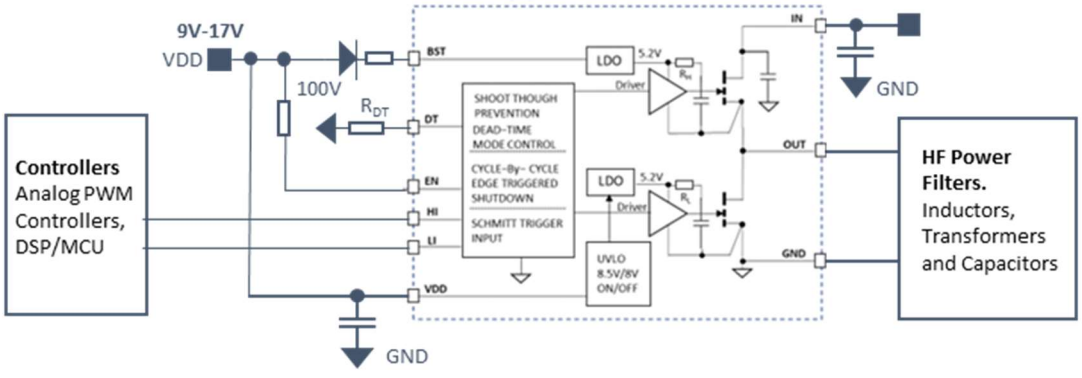
- DC/DC Brick Power
- Class-D Audio Amplifiers
- Low Inductance Motor Drive Inverter
- High Power Density Power Converters

Description

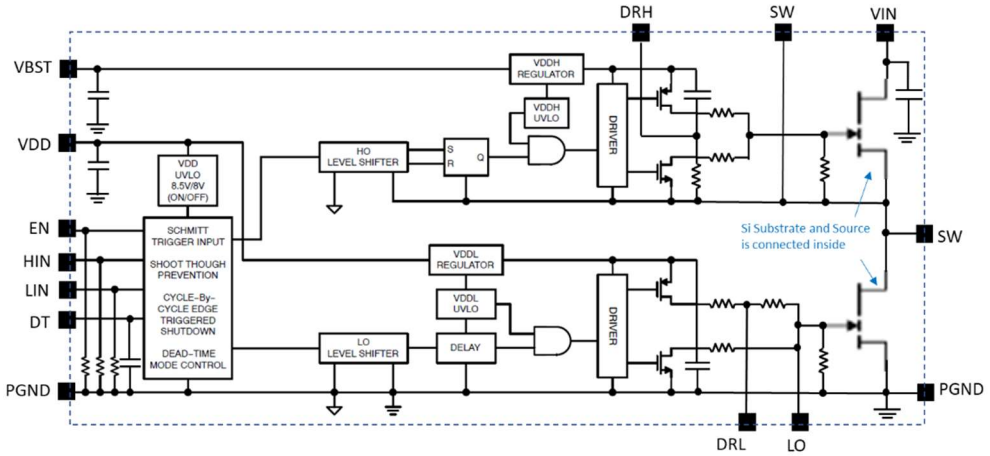
RT10 CIPS (Complete Integration Power Stage) Series are Fully Integrated GaN Half-Bridge power stages for multiple Applications in Fast Charger, High Power Density Switching Power, and Consumer segments. These CIPS are small-footprint, easy-to-design, and serve as a “drop-in” solution for board power. RT10 CIPS Series couples world-class GaN performance to Raytrons GaNCooling™ embedded modules that GaNCooling™ technology is a patented construction embeds all components without using bond wires, minimizing inductance, achieving ultra-low voltage spikes on gate and switch nodes, and minimizing RFI. The high dV/dt immunity, <1nH loop inductance and low thermal resistance to provides highest level of Power Density allowing designer simple, and quick to design high power density products.

Typical Application Circuit

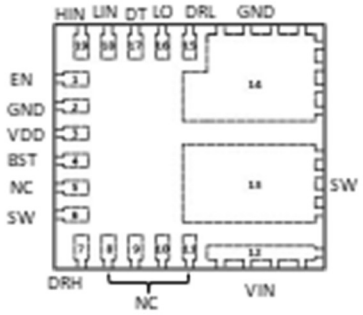
RT1002(5)SDH-DD can be designed in high power density power supply, including various DC/DC Brick Converters, Class-D Audio Amplifiers, Low Inductance Motor Driver and so on. Power loop (loop impedance from IN capacitor to PGND) PCB layout is critical, designer can refer to the PCB layout consideration section to selection dual-loop or thermal enhanced PCB layout for various applcations



Block Diagram



Pinout Table



Pinout		I/O Type	Description and Operation
#	Name		
1	EN	Input	Logic input for disabling the driver. Pulling the EN pin above 2.5 V maximum, enables the outputs, placing the module into an active ready state.
2, 14	GND	Power Ground	Connect to PCB Ground thru multiple Via's
3	VDD	Supply	Low side bias voltage. 9V to 17V operating rang.
4	BST	Supply	Floating high side bias voltage
5,8,9,10,11	NC	-	No Connection
6, 13	SW	Output	Half-Bridge power stage output (switching node)
7	DRH	Input	Option. Parallel a resistor between **DRH and SW** to speed up dv/dt falling time at SW node if necessary.
12	VIN	Power Input	Supply voltage to half-bridge power stage (buck-mode)
15	DRL	Output	Option. Parallel a resistor between **DRL and LO** to speed up dv/dt rising time at SW node if necessary
16	LO	Output	Low Side Gate
17	DT	Input	Dead time adjustment / mode selection
18	LIN	Input	Logic input for low−side gate driver output
19	HIN	Input	Logic input for high−side gate driver output

Absolute Maximum Ratings (T_{CASE} = 25 °C)

Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

- VIN to GND, VIN to SW, SW to GND ---------- 100V
- VDD to GND ---------- 18V
- Logic Input (HIN, LIN, EN) and DT ---------- VDD+0.3V
- LDR, LI, HI to GND ---------- 18V
- HDR, BST to GND ---------- 110V

Thermal Characteristics

The Surface Mount Device (SMD) with Bottom-side Cu Pads for Surface Mount PCB attach. $R_{\_JUNC-AMB}$ value based on recommended Via Pattern with multi-layer FR4 PCB. No Airflow (zero LFM) and no Top-side Heat Sink required to meet $R_{\_JUNC-AMB}$ (Conduction Heat Transfer). It is much more effective and competitive thermal design.

- Maximum Thermal Resistance (Junction to Board), R_{Θ_JB}, ---------- 1.0 °C/W
- Thermal Resistance (Junction to Ambient), R_{Θ_JA}, ---------- 8.4 °C/W
- Maximum Soldering Temperature (MSL3 rated), T_{Solder} ---------- 260°C

Normal Operation Conditions

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
Nominal VIN Range		V_{IN_Nom}	6.2		80	V	
Nominal SW Range		$SW_{\_Nom}$	0.9		80	V	
Nominal VDD Range		V_{DD_Nom}	9	12	17	V	
Nominal I/O Voltage		V_{IO_Nom}	2.5		17	V	
Nominal BST Range		$VBST_{\_Nom}$			SW+17	V	
Continuous I_{DS}	RT10005SDH-DD	I_{DS_Nom}		16		A	T_{JUN}=25°C
	RT10002SDH-DD			60			
Pulsed I_{DS}	RT10005SDH-DD	I_{DS_Pulse}		130		A	T_{JUN}=25°C, T_{PULSE}=300us
	RT10002SDH-DD			230			
Operating Temp		$T_{OPER.}$	-40		105	◦ C	

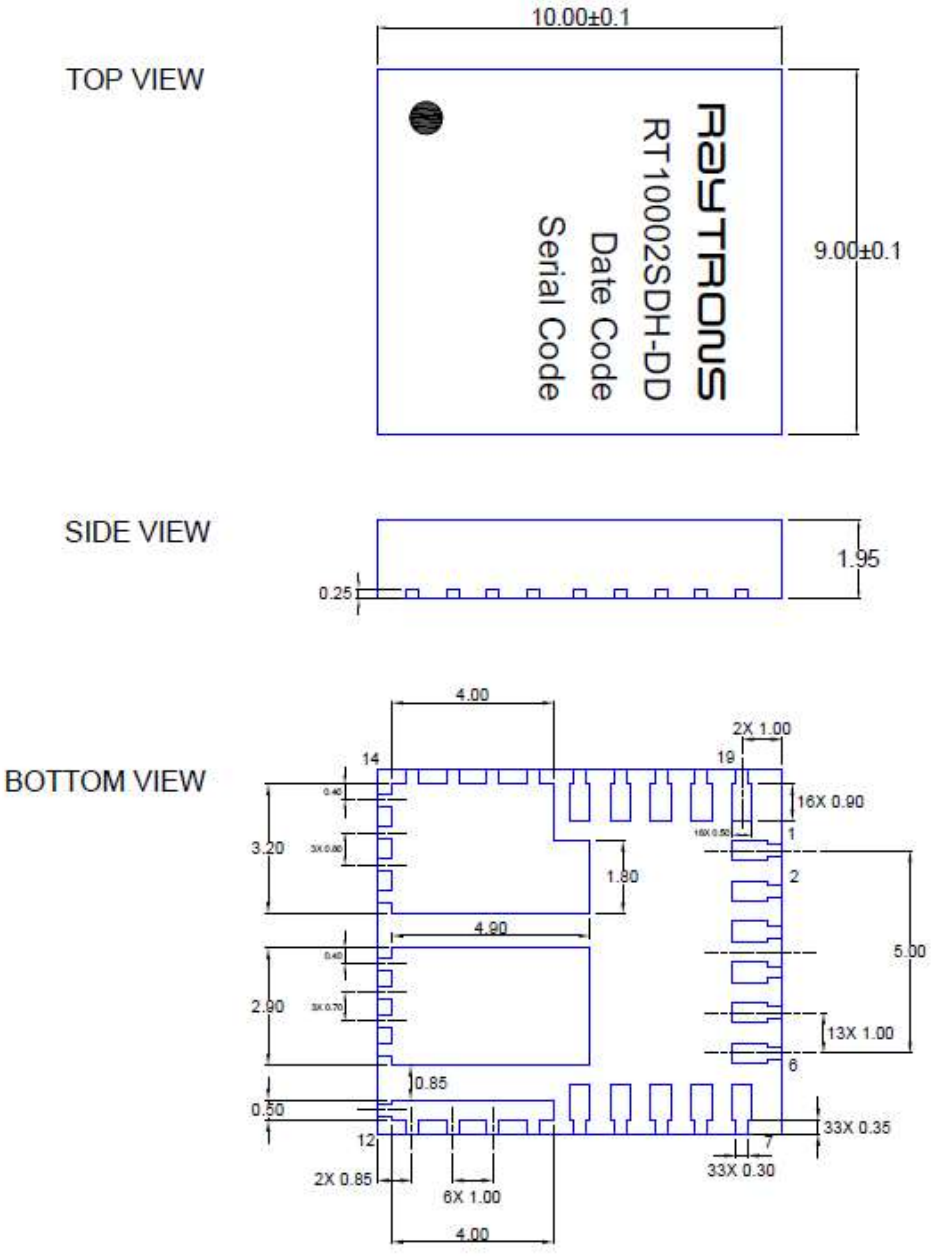
Electrical Specifications (T_{JUN}=25 Degrees of C)

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-Source On Resistance	RT10005SDH-DD	$R_{DS,ON}$		5.6	7	m Ω	H/S and L/S GaN Devices
	RT10002SDH-DD			2.4	3.2		
Source-Drain Forward Voltage	RT10005SDH-DD	V_{SD}		1.7		V	I_S = 0.5 A, V_{GS} = 0 V
	RT10002SDH-DD			1.5			
Input Capacitance	RT10005SDH-DD	C_{ISS}		767	1076	pF	V_{DS} = 50 V, V_{GS} = 0 V
	RT10002SDH-DD			1189	1570		
Reverse Transfer Capacitance	RT10005SDH-DD	C_{RSS}		3			
	RT10002SDH-DD			4.3			
Output Capacitance	RT10005SDH-DD	C_{OSS}		295	443		
	RT10002SDH-DD			562	843		

Source-Drain Recovery Charge	Q_{RR}		0		nC	
Gate Resistance	R_G		4.7		Ω	
Bootstrap capacitance	C_{BST}	80	100		nF	DC-Bias=0V
VDD capacitance	C_{VCC}	80	100		nF	DC-Bias=0V
Switching Frequency	F_{SW}	18		1000	kHz	
High Level Input Voltage Threshold	V_{INH}	-	-	2.5	V	
Low Level Input Voltage Threshold	V_{INL}	1.2	-	-	V	
Input Logic Voltage Hysteresis	$V_{IN,HYS}$		0.5		V	
Input Pull−down Resistance	R_{IN}		333		kΩ	V_{HIN} = V_{LIN} = 5 V
Minimum Dead−Time Control Voltage	$V_{DT,MIN}$	0.45	0.6	0.75	V	R_{DT} = 30 kΩ
	$t_{DT,MIN}$	22	30	38	ns	
Maximum Dead−Time Control Voltage	$V_{DT,MAX}$	3.1	4.0	4.8	V	R_{DT} = 200 kΩ
	$t_{DT,MAX}$	160	200	240	ns	
Dead−Time Disable Threshol	$V_{DT,0}$	0.35	0.4	0.45	V	Cross conduction prevention active
High− & Low−Side Overlap Enable Threshold	$V_{DT,OLE}$	5.5	6.0	6.5	V	Cross conduction prevention disabled
Propagation Delay	$T_{PD(H,L)}$			**TBD**	nsec	HI to SW, VIN=48V, and 10A I_{OUT}
Thermal Shunt Down	TSD	150			oC	Guaranteed by design, , is not tested in production.
Hysteresis of Thermal Shutdown	T_{HYS}		50		oC	
VDD Undervoltage-Lockout	$VDD_{,UVLO}$	8.0	8.5	9.0	V	VDD = Sweep
VDD Threshold Hysteresis	$VDD_{,HYS}$		0.5		V	
SW Rising Time	$T_{SW,R}$			**TBD**	nsec	VIN=48V, F_{SW}=500kHz and 10A I_{OUT}
SW Falling Time	$T_{SW,F}$			**TBD**	nsec	

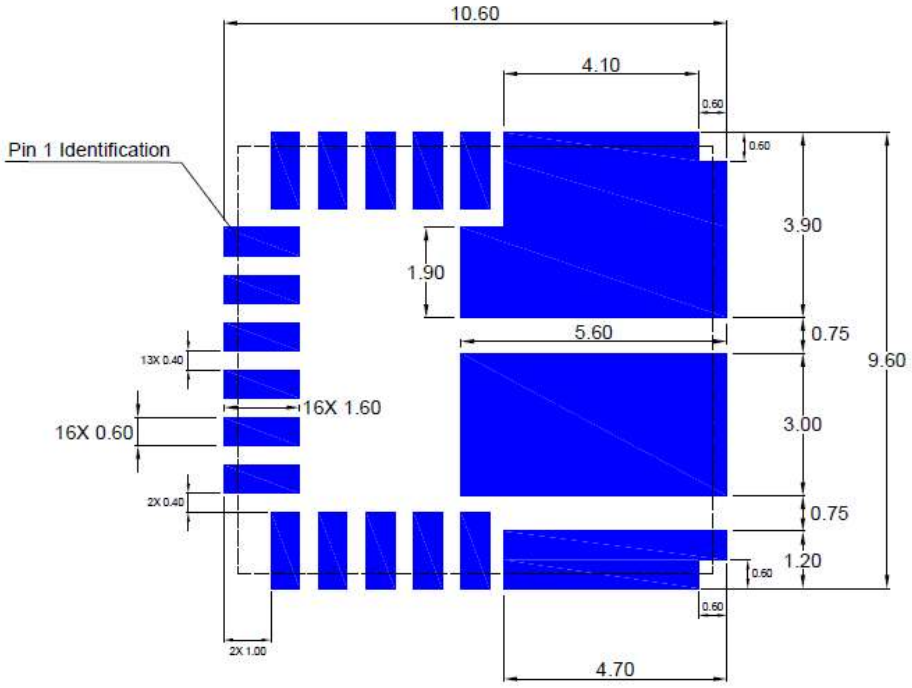
Application Specifications (TBD)

Package Outline： (QFN-SiP - 2 mm max height)

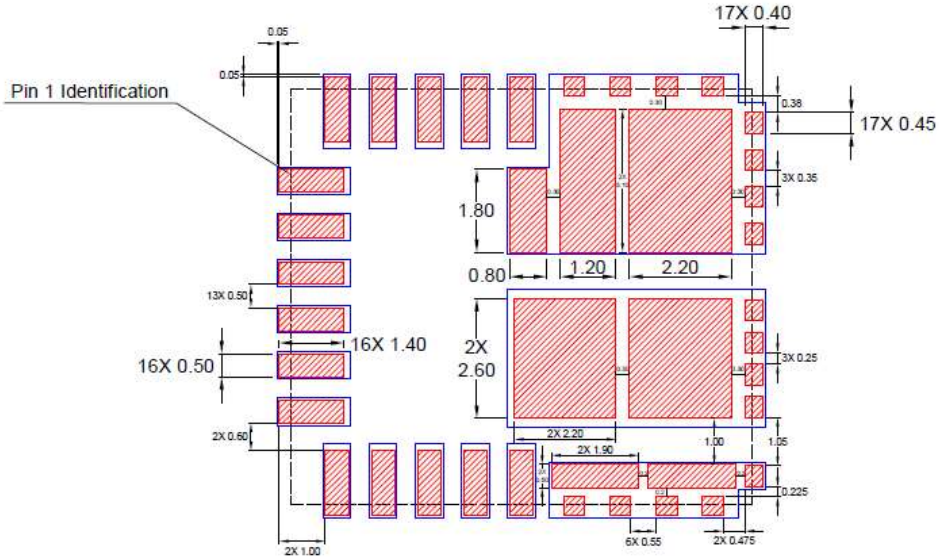


※:All dimensions are in units mm.
※:General tolerence is 0.05 mm unless otherwise noted.

Example Board Layout and Stencil Design：



RECOMMENDED LAND PATTERN



RECOMMENDED SOLDER PATTERN

※All dimensions are in units mm.
※53%~73% printed solder coverage by area under package.